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| 09/666,054 | 09/20/2000 | Sang Ho Lee | HI-017 | 5515 |

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| EXAMINER | |
|---|---|
| MOORE, IAN N | |
| **ART UNIT** | **PAPER NUMBER** |
| 2661 | |

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/666,054 | LEE, SANG HO | |
| | Examiner | Art Unit | |
| | Ian N. Moore | 2661 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5,7-12,14,15,17,19,20,22-27,29,31-33,39,40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,7-12,14,15,17,19,20 and 22-25* is/are allowed.

6)☒ Claim(s) *26,27,29,31-33,39,40,42 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The abstract discloses a legal phraseology "**means**" in line 10. Applicant is reminded of the proper language and format for an abstract of the disclosure. See MPEP § 608.01(b).

> The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

### *Claim Objections*

2. **Claim 43** has a status identifier of "currently amended"; however, it is noted that the claim 43 is newly added. Thus, claim 43 does not have a proper status identifier (i.e. New). See 37 CFR § 1.121 or 1.4.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 43 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claim 43** recites, "wherein **the ports** include:

**a first port** to inform the slave board of whether the master board is in the active State or Standby State;

**a second port** to inform the master board of whether the slave board is in the active or standby state;

**a third port** to output a reset signal from the master board to the slave board; and

**a fourth port** to receive a reset signal for resetting the master board " in lines 1-8.

1) It is unclear whether "the ports" belong to a master board, slave board, or both.

2) Note that "the first port", "the third port" and "forth port" appear be on the master board, and "a second port" appears to be on the slave board. However, in accordance with the specification and FIG. 3, it is appeared that each board has six ports. Thus, these inconsistent ports and their undefined corresponding boards make the claim unclear.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 39, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Uriu et al, hereinafter "Uriu", US Patent 5,301,184) in view of Blanc (US006411599B1). Uriu discloses a control system for switching duplicated switch units in an ATM exchange.

**With regard to claim 39**, Uriu discloses a first system including switch 21a is - operating as the active system (master board) and the second system including the switch 21 b is operating as the standby system (slave board) (column 5, lines 26-39). When the first system is switched from the active system to the standby system and the second system is switched from

the standby system to the active system, the active system information bit (state information / storing state information) "0" is written in each ATM cell applied to switch 21a (receiving state information) and the active system indication bit (state information / storing state information) "1" is written into each ATM cell applied to switch 21b (receiving state information) (column 6, lines 16-23). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (virtual path / virtual channel) (column 6, lines 36-39). With regard to claim 40, Uriu discloses a first system including switch 21a is operating as the active system (active state) and the second system including the switch 21b is operating as the standby system (standby state) (column 5, lines 26-39).

Uriu does not explicitly disclose transmitted through a pin-to-pin connection between the master and slave boards. However, Blanc teaches wherein the state information (see col. 3, line 10-65; control signals or watchdog information), is transmitted through a pin-to-pin connection between the master and slave boards (see FIG. 1, transmission through input to output port/pin connection 50i, 60, 40j between Switch Fabric left 10 and right 20; see col. 3, line 10 to col. 4, line 36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide input to output connections 50i, 60, 40 j between two switch fabrics, as taught by Blanc in the system of Uriu, so that it would provide fault tolerant mechanisms providing high availability of the switching resources; see Blanc col. 2, line 1-12.

**With regard to claim 40**, Uriu discloses a first system including switch 21a is operating as the active system (active state) and the second system including the switch 21b is operating as the standby system (standby state) (column 5, lines 26-39).

**With regard to claim 42**, Uriu discloses when the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal. Blanc et al discloses the switch fabric left 10 and right 20 are connected (connecting) to one another as illustrated by Figure 1 (see col. 3, line 10 to col. 4, line 36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide connection between fabrics to send control signals, as taught by Blanc in the system of Uriu, for the same motivation as stated above in claim 39.

5. Claims 26,27,29, and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uriu in view of (Matsurama et al, hereinafter "Matsurama", US Patent 6,269,077).

With regard to claim 26, Uriu discloses a first system including switch 21a is operating as the active system (master board) and the second system including the switch 21 b is operating as the standby system (slave) (column 5, lines 26-39). Connections between individual components of the active system and the second system, as illustrated by Figure 3, read on applicant's "at least one bus" (column 5, lines 14-26). Uriu further discloses a multiplexer or selector 27 connected to buffers 24a and 24b (connecting ports on master board and slave board) (column 5, lines 25-29). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (virtual path / virtual channel) (column 6, lines 36-39).

Uriu does not disclose wherein signal lines carry state information for switching duplexing between the two boards.

Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected to one another (signal lines) as illustrated by Figure 2 (column 5, lines 35-38). Matsumura et al further discloses that the system-switching control unit 21 or 31 performs control operation at the time of system switching over from the active to the standby system (column 4, lines 57-59).

A person of ordinary skill in the art would have been motivated to employ Matsumura in Uriu to provide a duplicated ATM switch that maintains delay qualities of the involved cells (Matsumura, column 2, lines 17-22). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Uriu and Matsumura (collectively "Uriu-Matsumura" so as to obtain the invention as specified in claim 26.

**With regard to claim 27**, Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected to one another (signal lines) as illustrated by Figure 2 (column 5, lines 35-38). As Figure 2 illustrates there are 2 connections (number of signal lines is more than 1) between system-switching control units 21 and 31.

**With regard to claim 29**, Uriu discloses when the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to

switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal.

**With further regard to claim 29**, Matsumura et al discloses a system switching control unit in both the active and standby units that are connected (connecting) to one another as illustrated by Figure 2 (column 5, lines 35-38). A signal that indicates a change in state is inherent and would read on applicant's reset signal.

**With regard to claim 31 and 32**, Uriu discloses a first system including switch 21a is operating as the active system and the second system including the switch 21b is operating as the standby system (column 5, lines 26-39). Figure 3 illustrates the components of both the active and the second system. Specifically, the each system comprises a switch 21a and 21b (at least one port), a demultiplexer 22a and 22b, a first buffer 23a and 23b (memory), a second buffer 24a and 24b (memory), a VPI/VCI table 25a and 25b (memory), and a monitor unit 26a and 26b (controller) (column 5, lines 14-26). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system the active system information bit (state information) "0" is written in each ATM cell applied to switch 21a and the active system indication bit (state information) "1" is written into each ATM cell applied to switch 21 b (column 6, lines 16-23). The monitor unit 26a changes (updates) the active system indication bit (controls duplexing state) related to first ATM cell stored in the VPI/VCI table 25a. The second buffer 24a refers to the contents of VPI/VCI table 25a and prevents the first ATM cell from being written therein (column 6, lines 36-41).

**With regard to claim 33**, Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected to one another (controller of slave monitors) as illustrated by Figure 2 (column 5, lines 35-38).

7. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uriu in view of Matsumura, as described above in claim 26, and further in view of Blanc and Dempsey (US006169726B1).

**Regarding Claim 43**, the combined system Uriu and Matsumura discloses all limitation as set forth above in claim 26. Uriu discloses informing the slave/master board whether the board is in the active of standby state (column 6, lines 5-23). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal. Thus, Uriu's active and standby system transmit/receive reset signals.

Matsumura discloses system-switching control units 21 and 31 in both the active and standby units that are connected (ports) to one another as illustrated by Figure 2 (column 5, lines 35-38). Matsumura et al further discloses that the system-switching control unit 21 or 31 performs control operation (whether a board is the first board or the second board / informs ... when master board is in standby state / request state information) at the time of system switching over from the active to the standby system (column 4, lines 57-59), and the control signals are

transmitted via the ports connecting the first and second boards (see FIG. 1, 4, Intersystem communication section 213; see col. 6, line 65 to col. 7, line 25). Thus, Matsumura active and standby units ports transmit/receive active/standby state indication signals.

Neither Uriu nor Matsumura explicitly discloses the plurality of ports (i.e. first, second, third, and fourth ports).

Blanc discloses the plurality of ports (first, second, third, and fourth ports) transmitting/receiving indication/status signals and reset signals (see FIG. 1, see col. 3, line 28-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the plurality of ports (first, second, third, and fourth ports) between two switch fabrics, as taught by Blanc in the system of Uriu, so that it would provide fault tolerant mechanisms providing high availability of the switching resources; see Blanc col. 2, line 1-12.

### *Allowable Subject Matter*

8. Claims 1-5,7-12,14,15,17,19,20,22-25 are allowed.

### *Response to Arguments*

9. Applicant's arguments, see pages 18-22, filed 12-16-2005, with respect to Claims 1-3,5,10-11,17,19,20,22-25 have been fully considered and are persuasive. The rejections of these claims have been withdrawn.

10. Applicant's arguments with respect to claims 26,27,29,31-33,39,40,42, and 43 have been considered but are moot in view of the new ground(s) of rejection.

**Regarding claims 26, the applicant argued that**, "...a number of signal lines connecting ports on the master board and slave board, wherein the signals lines carry state information for switching duplexing between boards. The Uriu and Matsumuara does not tech or suggest theses features...Moreover, claim 26 recites that the state information "indicates a virtual path and virtual channel for determining an active state and a standby state of the slave board and the master board." The Matsumura patent fails to teach or suggest theses features..." in page 23, paragraph 1-2.

**In response to applicant's argument, the examiner respectfully disagrees** with the argument above.

Matsumuara discloses a number of signal lines connecting ports on the master board and slave board (see FIG. 1, lines/ports between active and standby system), wherein the signals lines carry state information for switching duplexing between boards (column 5, lines 35-38; see col. 6, line 65 to col. 7, line 25; signal lines/ports transmit/receive control/state information). Uriu discloses a virtual path and virtual channel for determining an active state and a standby state of the slave board and the master board as set forth in above rejection.

**In response to applicant's arguments** against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the rejection is based upon the combined system of Uriu and Matsumura. Thus, the combined system of Uriu and Matsumura discloses the applicant claimed invention.

**Regarding claim 29, the applicant argued that,** "...state information includes a reset signal for resetting the master board when the master board switches to the standby state..." in page 23, paragraph 4.

**In response to applicant's argument, the examiner respectfully disagrees** with the argument above.

Uriu discloses informing the slave/master board whether the board is in the active of standby state (column 6, lines 5-23). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal. Thus, Uriu's active and standby system transmit/receive reset signals.

Matsumuara discloses the signals lines carry state information for switching duplexing between boards (column 5, lines 35-38; see col. 6, line 65 to col. 7, line 25; signal lines/ports transmit/receive control/state information).

Thus, the combined system of Uriu and Matsumuara discloses the applicant claimed invention.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that the combination of references as set forth in the 103 rejections is proper.

***Conclusion***

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
3-2-06

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